US 20100001266A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2010/0001266 A1**

(43) **Pub. Date: Jan. 7, 2010**

Ahn et al.

(54) **THIN FILM TRANSISTOR, METHOD OF FABRICATING THE SAME, AND ORGANIC LIGHT EMITTING DIODE DISPLAY DEVICE INCLUDING THE SAME**

(76) Inventors: **Ji-Su Ahn**, Yongin-City (KR); **Sung-Chul Kim**, Yongin-City (KR)

Correspondence Address:
LEE & MORSE, P.C.
3141 FAIRVIEW PARK DRIVE, SUITE 500
FALLS CHURCH, VA 22042 (US)

(21) Appl. No.: **12/458,142**

(22) Filed: **Jul. 1, 2009**

(30) **Foreign Application Priority Data**

Jul. 2, 2008 (KR) 10-2008-0064001

Publication Classification

(51) **Int. Cl.**
H01L 51/52 (2006.01)
H01L 29/786 (2006.01)
H01L 21/336 (2006.01)

(52) **U.S. Cl.** **257/40**; 257/66; 438/166; 257/E29.273; 257/E21.412; 257/E51.022

(57) **ABSTRACT**

A thin film transistor includes a substrate, a buffer layer on the substrate, a semiconductor layer on the buffer layer, a gate insulating layer on the semiconductor layer, a gate electrode on the gate insulating layer, an interlayer insulating layer on the entire surface of the substrate having the gate electrode, a first contact hole and a second contact hole, and source and drain electrodes on the interlayer insulating layer, insulated from the gate electrode, and having a portion connected with the semiconductor layer through the first contact hole. An organic light emitting diode display may include the thin film transistor along with a passivation layer on the entire surface of the substrate, and a first electrode, an organic layer, and a second electrode, which are on the passivation layer and electrically connected with the source and drain electrodes.

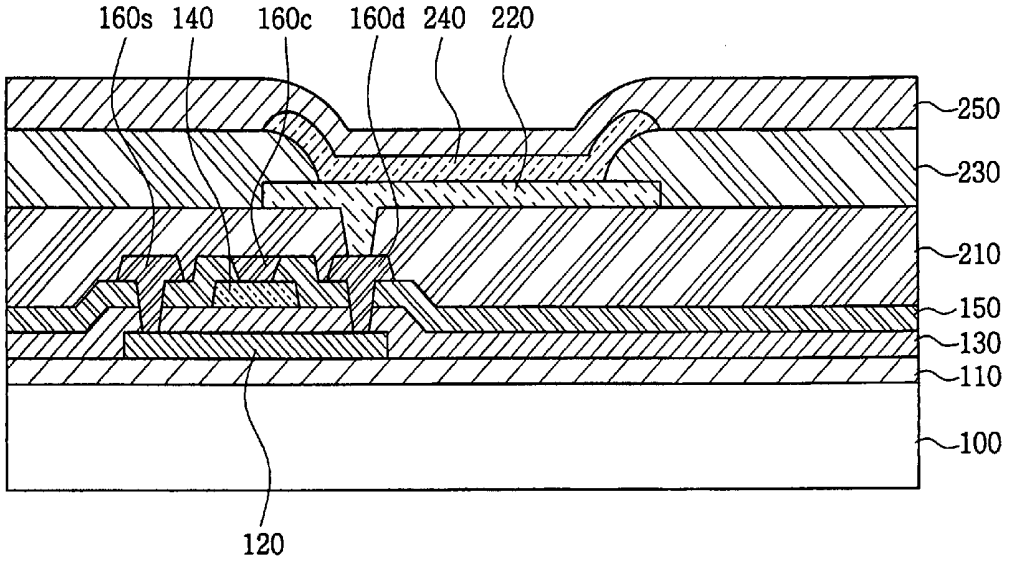


FIG.1A

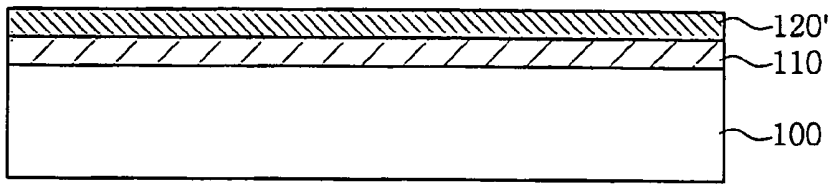


FIG.1B

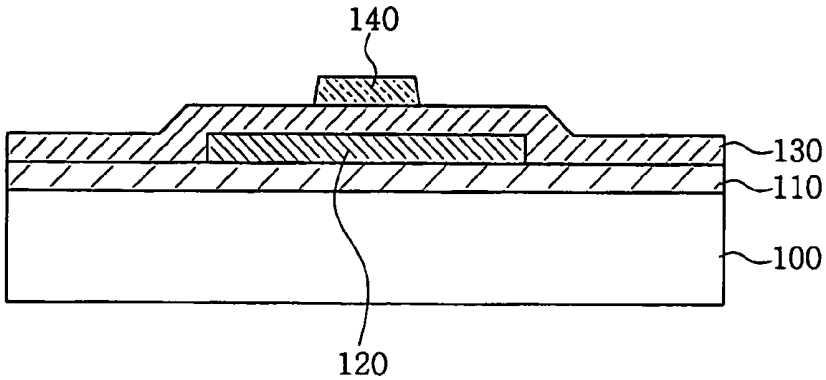


FIG.1C

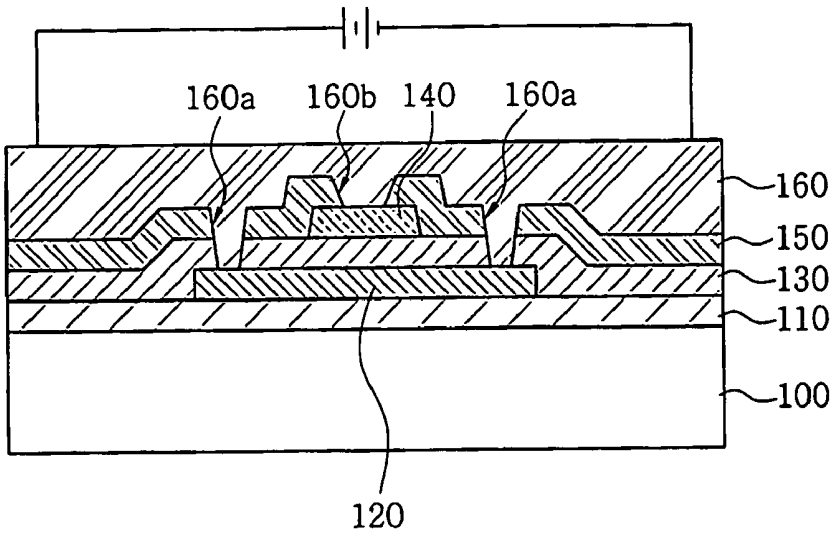

160a
160b
140
160a
160
150
130
110
100
120

FIG.1D

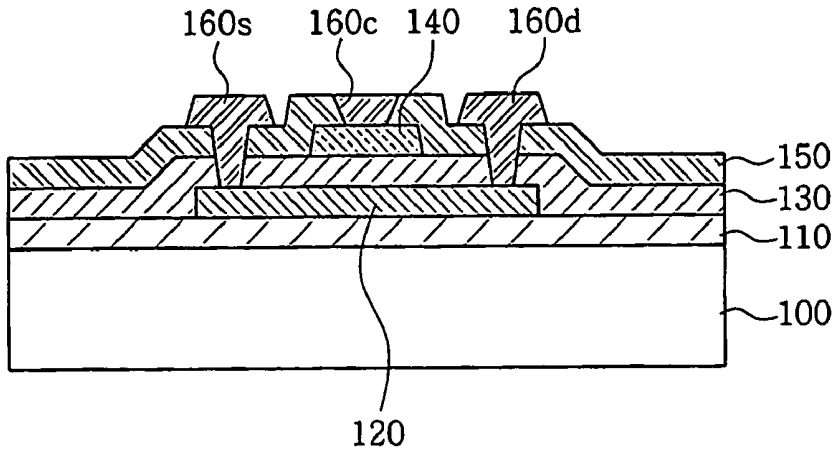

160s
160c
140
160d
150
130
110
100
120

FIG.2A

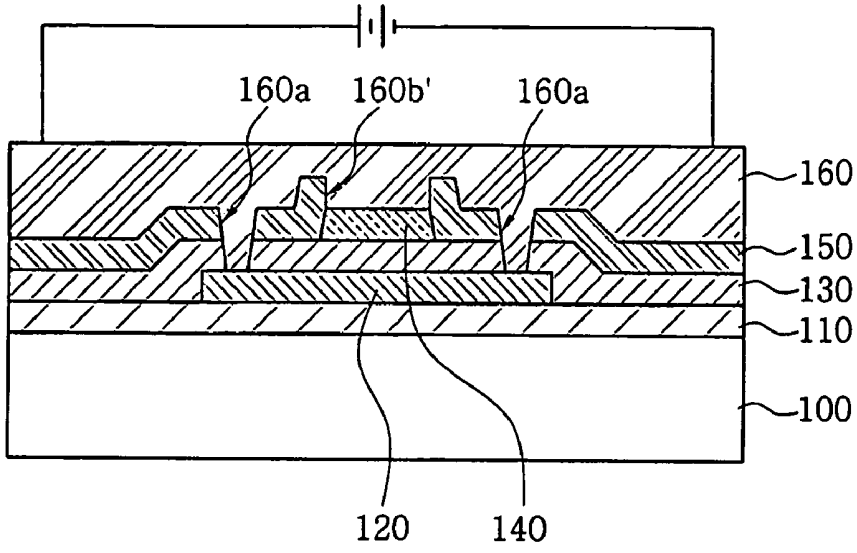

160a
160b'
160a
160
150
130
110
100
120
140

FIG.2B

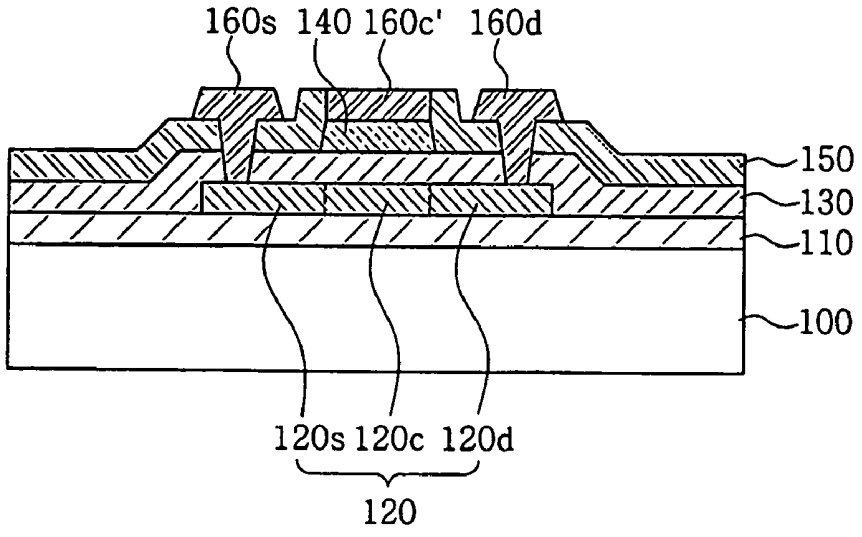
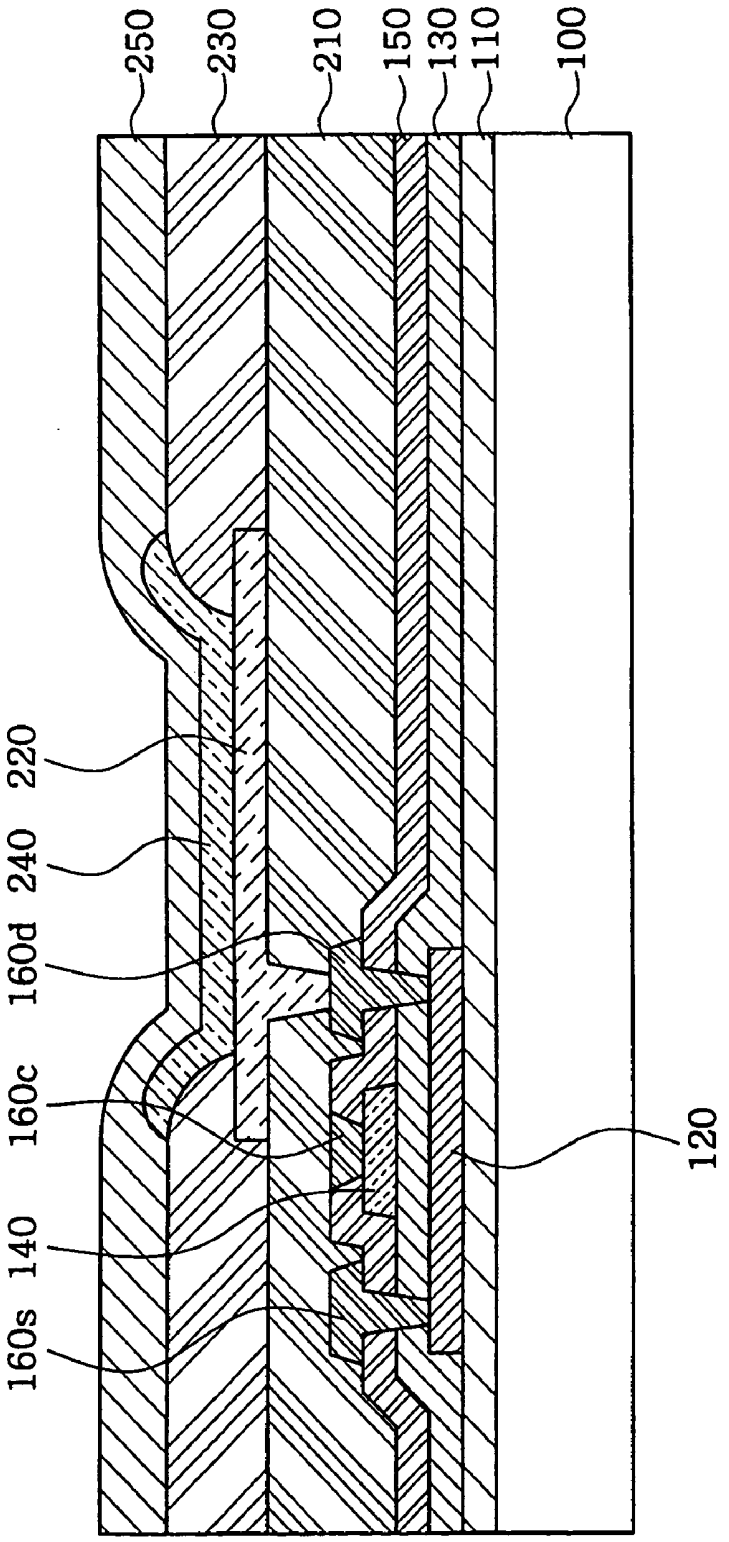

160s
140
160c'
160d
150
130
110
100
120s
120c
120d
120

FIG.3



THIN FILM TRANSISTOR, METHOD OF FABRICATING THE SAME, AND ORGANIC LIGHT EMITTING DIODE DISPLAY DEVICE INCLUDING THE SAME

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] Embodiments of the present invention relate to a thin film transistor, a method of fabricating the same, and an organic light emitting diode display device including the same. More particularly, embodiments of the present invention relate to a thin film transistor (TFT) that can prevent generated Joule heat from generating an arc during a conventional crystallization process.

[0003] 2. Description of the Related Art

[0004] Annealing methods used during a crystallization process generally include a furnace annealing method using a heat furnace, a rapid thermal annealing (RTA) method using radiant heat, e.g., a halogen lamp, a laser annealing method using a laser, and an annealing method using Joule heating. Among available annealing methods, an appropriate annealing method for the crystallization process is determined based on characteristics of material and process contemplated. Some of the factors to be considered in the selection of an appropriate annealing method are a range of an annealing temperature, uniformity of the annealing temperature, a heating rate, a cooling rate, purchase price, and maintenance cost. However, a selection of annealing method becomes very limited when high temperature annealing or high rate annealing only in a local region of a material is needed.

[0005] The laser annealing method can rapidly anneal a surface of a material. Despite this advantage, the laser annealing method has only limited applicability, since it can only be used to anneal particular materials. When scanned linear laser beams overlap to anneal a large-sized device, non-uniformity in intensity of the laser beam and in irradiation level of the laser beam may occur. Also, the laser annealing method requires very expensive equipment, as well as incurring high maintenance cost.

[0006] The RTA method is widely applied to a semiconductor fabrication process. However, with current technology, RTA methods can be applied only to a 300 mm silicon wafer, so it is difficult to uniformly anneal a substrate larger than 300 mm. Moreover, this method has a maximum heating rate of about 400° C./sec, and thus cannot be applied to a process requiring a higher heating rate than 400° C./sec.

[0007] Thus, research has been widely conducted on annealing methods to solve these problems and to eliminate processing limitations. A rapid annealing method, which applies an electrical field to a conductive layer and generates Joule heat, can rapidly anneal a selected material by transferring high heat. The rapid annealing method has much higher heating rate than that of the conventional RTA method. However, such a rapid annealing method cannot prevent physical defects of substrates from an arc generated during the Joule heating.

SUMMARY OF THE INVENTION

[0008] Embodiments of the present invention are therefore directed to a TFT, a method of fabricating the same, and an organic light emitting diode (OLED) display device using the same, which substantially overcome one or more of the disadvantages of the related art.

[0009] It is therefore a feature of an embodiment of the present invention to provide a TFT having a semiconductor layer crystallized by application of an electric field using a metal layer capable of preventing an arc formation during the crystallization of an amorphous layer, as the result of heat transfer from the metal layer.

[0010] It is therefore another feature of an embodiment of the present invention to provide a method of fabricating a TFT exhibiting above features and OLED display device including the TFT.

[0011] At least one of the above features and other advantages of the present invention may be realized by providing a TFT, including a substrate, a buffer layer on the substrate, a semiconductor layer on the buffer layer, a gate insulating layer on the semiconductor layer, a gate electrode on the gate insulating layer, an interlayer insulating layer on the entire surface of the substrate having the gate electrode, and having a first contact hole and a second contact hole, and source and drain electrodes on the interlayer insulating layer, insulated from the gate electrode, and having a portion connected with the semiconductor layer through the first contact hole.

[0012] It is therefore another feature of an embodiment of the present invention to provide the TFT including a metal layer forming source and drain electrodes further includes a metal layer pattern that disposes on the gate electrode.

[0013] It is therefore another feature of an embodiment of the present invention to provide the TFT having the first and the second contact holes in where the first contact hole is spaced apart from the second hole. The first contact hole partially exposes the semiconductor layer. The second contact hole partially exposes the gate electrode and is disposed in a region corresponding to a channel region of the semiconductor layer.

[0014] At least one of the above features and other advantages of the present invention may be realized by providing a method of fabricating the TFT including preparing a substrate, forming a buffer layer on the substrate, forming an amorphous semiconductor layer on the buffer layer, patterning the amorphous semiconductor layer to form a semiconductor layer pattern, forming a gate insulating layer on the semiconductor layer pattern, forming a gate electrode corresponding to the semiconductor layer pattern on the gate insulating layer, forming an interlayer insulating layer on the entire surface of the substrate, forming a first contact hole partially exposing the semiconductor layer, and a second contact hole partially exposing the gate electrode on the interlayer insulating layer, forming a metal layer on the entire surface of the substrate, applying an electrical field to the metal layer, and forming a semiconductor layer by crystallization of the semiconductor layer pattern and patterning the metal layer for source and drain electrodes to form source and drain electrodes insulated from the gate electrode and electrically connected with the semiconductor layer through the first contact hole.

[0015] It is therefore another feature of an embodiment of the present invention to provide the method of fabricating the TFT in where crystallization is performed while the metal layer is in contact with the gate electrode through the second contact hole.

[0016] It is therefore another feature of an embodiment of the present invention to provide the method of fabricating the TFT in where the electrical field of about 100 V/cm^2 to about 10,000 V/cm^2 is applied to the metal layer.

[0017] It is therefore another feature of an embodiment of the present invention to provide the method of fabricating the TFT in where the metal layer is formed to prevent exposure of the interlayer insulating layer. The voltage is applied to the metal layer.

[0018] It is therefore another feature of an embodiment of the present invention to provide the method of fabricating the TFT forming the first and second contact holes in where the first contact hole is formed to be spaced apart from the second contact hole. The second contact hole is formed to correspond to a channel region of the semiconductor layer.

[0019] Above feature and other advantages of the present invention may be realized by providing an OLED display device including a substrate, a buffer layer on the substrate, a semiconductor layer on the buffer layer, a gate insulating layer on the semiconductor layer, a gate electrode on the gate insulating layer; an interlayer insulating layer on the entire surface of the substrate having the gate electrode, and having a first contact hole and a second contact hole, source and drain electrodes on the interlayer insulating layer, insulated from the gate electrode, and having a portion connected with the semiconductor layer through the first contact hole, a passivation layer on the entire surface of the substrate, and a first electrode, an organic layer, and a second electrode, which are on the passivation layer and electrically connected with the source and drain electrodes.

[0020] It is therefore another feature of an embodiment of the present invention to provide the OLED display device including a metal layer forming source and drain electrodes further includes a metal layer pattern that disposes on the gate electrode.

[0021] It is therefore another feature of an embodiment of the present invention to provide the OLED display device including the first and the second contact holes in where the first contact hole is spaced apart from the second contact hole. The first contact hole partially exposes the semiconductor layer. The second contact hole partially exposes the gate electrode. In addition, the second contact hole is disposed in a region corresponding to a channel region of the semiconductor layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] The above and other features and advantages will become more apparent to those of ordinary skill in the art by describing in detail exemplary embodiments with reference to the attached drawings, in which:

[0023] FIGS. **1**A to **1**D illustrate cross-sectional views of stages in a method of making a TFT according to a first exemplary embodiment of the present invention;

[0024] FIGS. **2**A and **2**B illustrate cross-sectional views of stages in a method of making a TFT according to a second exemplary embodiment of the present invention; and

[0025] FIG. **3** illustrates a cross-sectional view of an OLED display device according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0026] Korean Patent Application No. 10-2008-0064001, filed on Jul. 2, 2008, in the Korean Intellectual Property Office, and entitled: "Thin Film Transistor, Method of Fabricating the Same, and Organic Light Emitting Diode Display Device Including the Same," is incorporated by reference herein in its entirety.

[0027] Embodiments will now be described more fully hereinafter with reference to the accompanying drawings, however, may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

[0028] In the drawing figures, the dimensions of layers and regions may be exaggerated for clarity of illustration. It will also be understood that when a layer or element is referred to as being "on" another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present. Further, it will be understood that when a layer is referred to as being "under" another layer, it can be directly under, and one or more intervening layers may also be present. In addition, it will also be understood that when a layer is referred to as being "between" two layers, it can be the only layer between the two layers, or one or more intervening layers may also be present. Like reference numerals refer to like elements throughout.

Exemplary Embodiment 1

[0029] FIGS. **1**A to **1**D illustrate cross-sectional views of a TFT according to a first exemplary embodiment of the present invention.

[0030] Referring to FIG. **1**A, a substrate **100** is provided. The substrate **100** may be formed of glass or plastic. A buffer layer **110** may be on the substrate **100**. The buffer layer **110** may prevent or reduce out-diffusion of moisture or impurities from the substrate **100** and/or may control a heat transfer rate during crystallization to facilitate the crystallization of an amorphous silicon layer. The buffer layer **110** may be, e.g., a silicon oxide layer, a silicon nitride layer, or a combination thereof.

[0031] Subsequently, an amorphous semiconductor layer **120'**, e.g., amorphous silicon, is formed on the substrate **100** and then patterned, thereby forming a semiconductor layer pattern **120***a* (shown in FIG. **1**B) to be used as a semiconductor layer **120** (shown in FIG. **1**C).

[0032] Then, referring to FIG. **1**B, a gate insulating layer **130** may be provided on the entire surface of the substrate **100** including the semiconductor layer pattern **120***a*. The gate insulating layer **130** may be a silicon oxide layer, a silicon nitride layer, or a combination thereof.

[0033] A gate electrode **140** may be formed on the gate insulating layer **130** to correspond to the semiconductor layer pattern **120***a*. The gate electrode **140** may be formed of a single layer, e.g., aluminum (Al), an Al alloy such as aluminum-neodymium (Al—Nd), etc., or a multi layer formed by stacking, e.g., an aluminum (Al) alloy on chromium (Cr) or molybdenum (Mo) alloy.

[0034] Referring to FIG. **1**C, an interlayer insulating layer **150** may be formed on the entire surface of the substrate. The interlayer insulating layer **150** may be a silicon oxide layer, a silicon nitride layer, or a combination thereof.

[0035] After forming the interlayer insulating layer **150**, first and second contact holes **160***a* and **160***b* may be formed. The first contact hole **160***a* may be formed by partially etching the gate insulating layer **130** and the interlayer insulating layer **150** to partially expose the semiconductor layer pattern **120***a*. The second contact hole **160***b* may be formed by partially etching the interlayer insulating layer **150** on the gate electrode **140** to partially expose the gate electrode.

[0036] A metal layer **160** may be formed on the entire surface of the substrate **100**. When the metal layer **160** is heated by application of an electrical field, heat generated from the metal layer **160** is transferred to the underlying semiconductor layer pattern **120***a*, which is then crystallized into the semiconductor layer **120**, e.g., polycrystalline silicon.

[0037] The metal layer **160** is connected to the semiconductor layer **120** through the first contact hole **160***a*, preventing formation of an arc during the crystallization and reducing defects thereof. Also, the metal layer **160** may be connected to the gate electrode **140** through the second contact hole **160***b*, transferring heat generated from the metal layer **160** to the underlying semiconductor layer **120** through the gate electrode **140**, facilitating crystallization.

[0038] Here, for preferable crystallization, an electrical field of about 100 V per unit area (cm^2) to about 10,000 V per unit area (cm^2) may be applied for about 1 μs to about 1 sec. An electrical field of less than about 100 V per unit area (cm^2) cannot generate sufficient Joule heat for crystallization, while an electrical field of more than 10,000 V per unit area (cm^2) can generate a local arc. Further, when an electrical field is applied for less than 1 μs, crystallization may not be facilitated due to insufficient Joule heat, while when an electrical field is applied for more than 1 sec, the substrate may be bent or may form a defect along an edge due to heat transfer during crystallization.

[0039] Referring to FIG. **1**D, after the semiconductor layer **120** is formed, the metal layer **160** may be patterned to form source and drain electrodes **160***s* and **160***d*. Here, a metal layer pattern **160***c* may remain in the second contact hole **160***b* on the gate electrode **140**. Accordingly, the TFT according to an Exemplary embodiment 1 is completed.

[0040] The metal layer **160** is generally formed to a thickness suitable for the source and drain electrodes **160***s* and **160***d*, e.g., about 50 nm to about 200 nm. When the thickness of the metal layer **160** is less than about 50 nm, the metal layer **160** on the gate electrode **140** may not be uniform, so that heat cannot be uniformly transferred to the amorphous silicon layer, resulting in non-uniform crystallization. When the thickness of the metal layer **160** is greater than about 200 nm, the gate electrode **140** may no longer be suitable for thin film device. Thus, when the metal layer **160** has a thickness of about 200 nm or less, but exceeding 50 nm, uniform crystallization may be realized, while allowing the gate electrode to properly operate as an electrode suitable for the thin film device.

[0041] The metal layer **160** may be formed of one or more of molybdenum (Mo), chromium (Cr), tungsten (W), MoW, aluminum (Al), Al—Nd, titanium (Ti), titanium nitride (TiN), copper (Cu), a Mo alloy, an Al alloy and a Cu alloy.

Exemplary Embodiment 2

[0042] Exemplary embodiment 2 is almost same as Exemplary embodiment 1 except for formation of a second contact hole. Thus, descriptions thereof may not be repeated.

[0043] Referring to FIG. **2**A, by the same method described with references to FIGS. **1**A and **1**B in Exemplary embodiment **1**, the substrate **100**, the buffer layer **110**, the semiconductor layer pattern **120***a*, e.g., amorphous silicon pattern, the gate insulating layer **130**, and the gate electrode **140** are formed. Then, an interlayer insulating layer **150** may be formed on the entire surface of the substrate **100**.

[0044] Next, the first contact hole **160***a* and a second contact hole **160***b*' may be formed by etching. The gate insulating layer **130** and the interlayer insulating layer **150** may be partially etched, thereby forming the first contact hole **160***a* and partially exposing the semiconductor layer pattern **120***a* through the first contact hole **160***a*. The second contact hole **160***b*' may be formed by partially etching the interlayer insulating layer **150**, which further results in partially exposing the gate electrode **140**.

[0045] A region of the gate electrode **140** exposed through the second contact hole **160***b*' corresponds to a channel region **120***c* of the semiconductor layer **120** (shown in FIG. **2**B) to be formed later. When the second contact hole **160***b*' is formed as described above, a contact area between the metal layer **160** and the gate electrode **140** is formed above the channel region **120***c* of the semiconductor layer **120** (shown in FIG. **2**B). Such placement of the contact area results in effective heat transfer to the channel region, and crystallization of the channel region.

[0046] After the metal layer **160** is formed on the entire surface of the substrate **100**, the semiconductor layer pattern **120***a* is crystallized into the semiconductor layer **120** by the same method as described in Exemplary embodiment **1**.

[0047] Referring to FIG. **2**B, the metal layer **160** is patterned by the same method as described in Exemplary embodiment **1**, thereby forming source and drain electrodes **160***s* and **160***d*. Here, a metal layer pattern **160***c*' may remain on the gate electrode **140** in the second contact hole **160***b*'. Accordingly, the TFT according to Exemplary embodiment **2** is completed.

[0048] FIG. **3** illustrates a cross-sectional view of an OLED display device having a TFT according to an embodiment. The TFT is the same as that described in Exemplary embodiment **1**.

[0049] Referring to FIG. **3**, a passivation layer **210** may be formed on the entire surface of the substrate **100** including the TFT according to the exemplary embodiment described in FIG. **1**D. The passivation layer **210** may be formed of an inorganic material, e.g., silicon oxide, silicon nitride, and silicate on glass, an organic material, e.g., polyimide, benzocyclobutene series resin and acrylate, or a combination thereof.

[0050] The passivation layer **210** may be etched to form a via hole exposing the source electrode **160***s* or drain electrode **160***d*. A first electrode **220** connected to one of the source and drain electrodes **160***s* and **160***d* through the via hole may be formed. The first electrode **220** may be an anode or a cathode. When the first electrode **220** is an anode, it may be formed of a transparent conductive layer, e.g., an ITO, IZO, or ITZO layer. When the first electrode **220** is a cathode, it may be formed of magnesium (Mg), calcium (Ca), aluminum (Al), silver (Ag), barium (Ba), or an alloy thereof.

[0051] Next, a pixel defining layer **230** may be formed on the passivation layer **210** and on the first electrode **220**. The pixel defining layer may include an opening partially exposing surface of the first electrode **220** and an organic layer **240** including an emission layer, formed on the exposed portion of the first electrode **220**. The organic layer **240** may further include at least one or more of a hole injection layer, a hole transport layer, a hole blocking layer, an electron blocking layer, an electrode injection layer, and an electron transport layer. Then, a second electrode **250** may be formed on the

pixel defining layer **230** and on the organic layer **240**. Accordingly, the OLED display device according to an exemplary embodiment is completed.

[0052] By forming the electrode on the amorphous semiconductor before crystallization, an occurrence of an arc caused by Joule heat during the crystallization may be prevented. Thus, defects can be reduced, and production yield can be improved.

[0053] Exemplary embodiments of the present invention have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. Accordingly, it will be understood by those of ordinary skill in the art that various changes in form and details may be made without departing from the spirit and scope of the present invention as set forth in the following claims.

What is claimed is:

1. A thin film transistor (TFT), comprising:
- a substrate;
- a buffer layer on the substrate;
- a semiconductor layer on the buffer layer;
- a gate insulating layer on the semiconductor layer;
- a gate electrode on the gate insulating layer;
- an interlayer insulating layer on the entire surface of the substrate having the gate electrode, and having a first contact hole and a second contact hole; and
- source and drain electrodes on the interlayer insulating layer, insulated from the gate electrode, and having a portion connected with the semiconductor layer through the first contact hole.

2. The TFT as claimed in claim **1**, further comprising:
- a metal layer pattern for source and drain electrodes disposed on the gate electrode.

3. The TFT as claimed in claim **1**, wherein the first contact hole is spaced apart from the second contact hole.

4. The TFT as claimed in claim **1**, wherein the first contact hole partially exposes the semiconductor layer.

5. The TFT as claimed in claim **1**, wherein the second contact hole partially exposes the gate electrode.

6. The TFT as claimed in claim **1**, wherein the second contact hole is disposed in a region corresponding to a channel region of the semiconductor layer.

7. A method of fabricating a thin film transistor, comprising:
- preparing a substrate;
- forming a buffer layer on the substrate;
- forming an amorphous semiconductor layer on the buffer layer;
- patterning the amorphous semiconductor layer to form a semiconductor layer pattern;
- forming a gate insulating layer on the semiconductor layer pattern;
- forming a gate electrode corresponding to the semiconductor layer pattern on the gate insulating layer;
- forming an interlayer insulating layer on the entire surface of the substrate;
- forming a first contact hole partially exposing the semiconductor layer, and a second contact hole partially exposing the gate electrode on the interlayer insulating layer;
- forming a metal layer on the entire surface of the substrate;
- applying an electrical field to the metal layer and forming a semiconductor layer by crystallization of the semiconductor layer pattern; and
- patterning the metal layer for source and drain electrodes to form source and drain electrodes insulated from the gate electrode and electrically connected with the semiconductor layer through the first contact hole.

8. The method as claimed in claim **7**, wherein crystallization is performed while the metal layer is in contact with the gate electrode through the second contact hole.

9. The method as claimed in claim **7**, wherein the electrical field is about 100 V/cm^2 to about 10,000 V/cm^2.

10. The method as claimed in claim **7**, wherein the metal layer is formed to prevent exposure of the interlayer insulating layer, and the voltage is applied thereto.

11. The method as claimed in claim **7**, wherein the first contact hole is formed to be spaced apart from the second contact hole.

12. The method as claimed in claim **7**, wherein the second contact hole is formed to correspond to a channel region of the semiconductor layer.

13. An organic light emitting diode (OLED) display device, comprising:
- a substrate;
- a buffer layer on the substrate;
- a semiconductor layer on the buffer layer;
- a gate insulating layer on the semiconductor layer;
- a gate electrode on the gate insulating layer;
- an interlayer insulating layer on the entire surface of the substrate having the gate electrode, and having a first contact hole and a second contact hole;
- source and drain electrodes on the interlayer insulating layer, insulated from the gate electrode, and having a portion connected with the semiconductor layer through the first contact hole;
- a passivation layer on the entire surface of the substrate; and
- a first electrode, an organic layer, and a second electrode, which are on the passivation layer and electrically connected with the source and drain electrodes.

14. The OLED display device as claimed in claim **13**, further comprising:
- a metal layer pattern for source and drain electrodes disposed on the gate electrode.

15. The OLED display device as claimed in claim **13**, wherein the first contact hole is spaced apart from the second contact hole.

16. The OLED display device as claimed in claim **13**, wherein the first contact hole partially exposes the semiconductor layer.

17. The OLED display device as claimed in claim **13**, wherein the second contact hole partially exposes the gate electrode.

18. The OLED display device as claimed in claim **13**, wherein the second contact hole is disposed in a region corresponding to a channel region of the semiconductor layer.

* * * * *

专利名称(译)	薄膜晶体管，其制造方法以及包括该薄膜晶体管的有机发光二极管显示装置		
公开(公告)号	US20100001266A1	公开(公告)日	2010-01-07
申请号	US12/458142	申请日	2009-07-01
[标]申请(专利权)人(译)	AHN苏姬 金圣CHUL		
申请(专利权)人(译)	AHN JI-SU 金成哲		
当前申请(专利权)人(译)	AHN JI-SU 金成哲		
[标]发明人	AHN JI SU KIM SUNG CHUL		
发明人	AHN, JI-SU KIM, SUNG-CHUL		
IPC分类号	H01L51/52 H01L29/786 H01L21/336		
CPC分类号	H01L21/02532 H01L21/02667 H01L27/1281 H01L29/66757 H01L27/124 H01L27/3262		
优先权	1020080064001 2008-07-02 KR		
外部链接	Espacenet USPTO		

摘要(译)

薄膜晶体管包括基板，基板上的缓冲层，缓冲层上的半导体层，半导体层上的栅极绝缘层，栅极绝缘层上的栅极，整个表面上的层间绝缘层所述基板具有所述栅电极，第一接触孔和第二接触孔，以及所述层间绝缘层上的源电极和漏电极，与所述栅电极绝缘，并且具有通过所述第一接触孔与所述半导体层连接的部分。有机发光二极管显示器可以包括薄膜晶体管以及在基板的整个表面上的钝化层，以及第一电极，有机层和第二电极，它们位于钝化层上并且与第一电极，有机层和第二电极电连接。源极和漏极。